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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,426	07/12/2002	Nai-Shung Chang	7983-US-PA	9334

31561 7590 02/24/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,426	CHANG ET AL.	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election *without traverse* of Group I, claims 1-28, in Paper No. 4, is acknowledged. Non-elected claims 29-39 have been canceled.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Abstract

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The

disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations: the layout structure placed in an area where is between a control chip and the CPU, a top signal layer, a first signal line, a reference potential providing layer located below the top signal layer, a power layer located below the reference potential providing layer, a voltage providing area, a reference potential providing area, a bottom signal layer, pin grid array, ball grid array, a mother board, the other element besides the CPU, a third area, a third signal line, a plurality of power cut areas, a fourth signal line, a first reference layer having a first reference potential, a second reference layer, a first reference area having the first reference potential, a second reference area having a second reference potential, a second signal layer, a second area, a third signal layer, a third reference layer having said first reference potential, a fourth reference layer, a third reference area having the first reference potential, a fourth reference area having the second reference potential, a fourth signal layer, a third area, a fifth signal layer, a fifth reference layer having the first reference potential, a sixth reference layer having a plurality of reference areas that have a plurality of other reference potentials, a sixth signal layer, in claims 1-28 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims **2-3** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims **1 and 8**, the phrase "*the first signal line **refers** to the reference potential providing layer*" is unclear as to whether it implies a connection, a coupling or any relationship between the first signal line and the reference potential providing layer.

In claims **1 and 8**, the phrase "*the second signal line **refers** to the reference potential providing area*" is unclear as to whether it implies a connection, a coupling or any relationship between the first signal line and the reference potential providing area.

In claim **14**, the phrase "*the third signal line **refers** to the reference potential providing layer*" is unclear as to whether it implies a connection, a coupling or any relationship between the third signal line and the reference potential providing layer.

In claim **15**, the phrase "*the first signal line... **refers** to the first reference layer*" is unclear as to whether it implies a connection, a coupling or any relationship between the first signal line and the first reference layer.

In claim **15**, the phrase "*the second signal line... **refers** to the first reference area*" is unclear as to whether it implies a connection, a coupling or any relationship between the second signal line and the first reference area.

In claim **21**, lines 1-4, the phrase "*A motherboard ... comprising: a first area, wherein said whole CPU is placed in* ***said range*** *of said first area,* ***said stack structure*** *of said first area along a first direction sequentially comprising:*" is unclear as to what range that "*said range*" implies, and what the stack structure that the "*said stack structure*" implies.

In claim **23**, the phrase "*the plurality of signals that are placed on the second signal layer and the fourth signal layer* ***refer*** *to the first reference area and the third reference area*" is unclear as to whether it implies a connection, a coupling or any relationship between the signals and the reference areas.

In claim **24**, the phrase "*the plurality of signals... **refer** to the first reference potential*" is unclear as to whether it implies a connection, a coupling or any relationship between the signals and the first reference potential.

In claim **21**, the limitations "*said range*" and "*said stack structure*" in lines 3-4, "*said range of said second area*" and "*said stack structure of said second area*" in lines 13-14, and "*said range of said third area*" and "*said stack structure of said third area*" in lines 22-23, have no antecedent basis.

Claims **2-7, 9-14, 16-20** and **22-28** are rejected since they include the limitations of one of claims **1, 8, 15 and 21**.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-28, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art of figure 1 ("the Prior Art") in view of Govind et al. (6,531,932).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-2, 5-9, 12-24 and 27-28, the Prior Art discloses all the limitations of the claimed invention as described in Applicant's Specification, sections [0004], [0005], [0006], [0007], [0008], but it fails to teach: a) one grounded layer only located below the top signal layer, b) a bottom signal layer located below the power layer (instead of being formed between two grounded layers).

Govind et al. while related to a similar printed circuit board design teach (see specifically figure 1) a printed circuit board (12) comprising a top signal layer (14), a grounded layer (16) located below the top signal layer, a power layer (18) located below the grounded layer, and a bottom signal layer (20) located below the power layer (18), in order to provide voltage potentials and input/output signals to the semiconductor device, such as the device (22), mounted thereon. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the printed circuit board in the Prior Art by applying the printed circuit board having signal and power layers, as taught by Govind et

al, for the purpose of having a signal layer at the bottom of the circuit board and reducing the thickness of the circuit board.

Regarding claims 3-4, 10-11, and 25-26, the proposed device of the Prior Art and Govind et al. discloses all the limitations of the claimed invention as detailed above except for specifying the locations of the reference potential providing area (e.g., nearest to the CPU) and the CPU operating voltage providing area (e.g., a contiguous side of the side nearest to the CPU). It would have been obvious to one of ordinary skill in the art at the time the invention was made to rearrange the locations of *the reference potential providing area* and *the CPU operating voltage providing area* as claimed, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re* Japikse, 86 USPQ 70.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211 (after 2/05/2004 the phone number would be changed to 571-272-1935). The examiner can normally be reached on 6:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
January 30, 2004